SystemVerilog for Design Second Edition

Stuart Sutherland, Simon Davidmann, Peter Flake

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SystemVerilog is a rich set of extensions to the IEEE 1364-2001 Verilog Hardware Description Language (Verilog HDL). These extensions address two major aspects of HDL-based design. First, modeling very large designs with concise, accurate, and intuitive code. Second, writing high-level test programs to efficiently and effectively verify these large designs. The first edition of this book addressed the first aspect of the SystemVerilog extensions to Verilog. Important modeling features were presented, such as two-state data types, enumerated types, user-degined types, structures, unions, and interfaces. Emphasis was placed on the proper usage of these enhancements for simulation and synthesis. SystemVerilog for Design, Second Edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard. It is important that the book reflect these syntax and semantic changes to the SystemVerilog language. In addition, the second edition features a new chapter that explanis the SystemVerilog 'packages', a new appendix that summarizes the synthesis guidelines presented throughout the book, and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys, Mentor, and Cadance tools.

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